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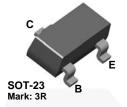


March 2014

# MMBT5771 PNP Switching Amplifier

# **Description**

This device is designed for very high-speed, saturated switching at collector currents to 100 mA. Sourced from process 65.



# **Ordering Information**

Part Number	Marking	Package	Packing Method	
MMBT5771	3R	SOT-23 3L	Tape and Reel	

# **Absolute Maximum Ratings**(1),(2)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at  $T_A = 25^{\circ}$ C unless otherwise noted.

Symbol	Parameter	Value	Unit
V <sub>CEO</sub>	Collector-Emitter Voltage	-15	V
$V_{CBO}$	Collector-Base Voltage	-15	V
V <sub>EBO</sub>	Emitter-Base Voltage	-4.5	V
I <sub>C</sub>	Collector Current - Continuous	-200	mA
$T_{J}$ , $T_{STG}$	Junction and Storage Temperature Range	-55 to +150	°C

#### Notes:

- 1. These ratings are based on a maximum junction temperature of 150°C.
- These are steady-state limits. Fairchild Semiconductor should be consulted on applications involving pulsed or low-duty-cycle operations.

# Thermal Characteristics(3)

Values are at  $T_A = 25$ °C unless otherwise noted.

Symbol	Parameter	Max.	Unit
D_	Total Device Dissipation	225	mW
$P_{D}$	Derate Above T <sub>A</sub> = 25°C	1.8	mW/°C
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	556	°C/W

#### Note:

3. Device mounted on FR-4 PCB 1.6 inch X 1.6 inch X 0.06 inch.

# **Electrical Characteristics**

Values are at  $T_A = 25^{\circ}C$  unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V <sub>(BR)CEO</sub>	Collector-Emitter Breakdown Voltage <sup>(4)</sup>	I <sub>C</sub> = -3.0 mA, I <sub>B</sub> = 0	-15		V
V <sub>(BR)CES</sub>	Collector-Emitter Breakdown Voltage	$I_C = -100  \mu A,  V_{BE} = 0$	-15		V
V <sub>(BR)CBO</sub>	Collector-Base Breakdown Voltage	$I_C = -100 \mu\text{A}, I_E = 0$	-15		V
V <sub>(BR)EBO</sub>	Emitter-Base Breakdown Voltage	I <sub>E</sub> = -100 μA, I <sub>C</sub> = 0	-4.5		V
I <sub>CBO</sub>	Collector Cut-Off Current	V <sub>CB</sub> = -8.0 V, I <sub>E</sub> = 0		-10	nA
		$V_{CE} = -8.0 \text{ V}, V_{BE} = 0$		-10	nA
I <sub>CES</sub>	Collector Cut-Off Current	V <sub>CE</sub> = -8.0 V, V <sub>BE</sub> = 0, T <sub>A</sub> = 125°C		-5.0	μА
I <sub>EBO</sub>	Emitter Cut-Off Current	$V_{EB} = -4.5 \text{ V}, I_{C} = 0$		-1.0	μΑ
		$I_C = -1.0 \text{ mA}, V_{CE} = -0.5 \text{ V}$	35		
		$I_C = -10 \text{ mA}, V_{CE} = -0.3 \text{ V}$	50	120	
h <sub>FE</sub>	DC Current Gain <sup>(4)</sup>	$I_C$ = -10 mA, $V_{CE}$ = -0.3 V, $T_A$ = -55°C	20		
		$I_C = -50 \text{ mA}, V_{CE} = -1.0 \text{ V}$	40		
	Collector-Emitter Saturation Voltage <sup>(4)</sup>	$I_C = -1.0 \text{ mA}, I_B = -0.1 \text{ mA}$		-0.15	V
V <sub>CE</sub> (sat)		$I_C = -10 \text{ mA}, I_B = -1.0 \text{ mA}$		-0.18	
		$I_C = -50 \text{ mA}, I_B = -5.0 \text{ mA}$		-0.60	
	Base-Emitter Saturation Voltage <sup>(4)</sup>	$I_C = -1.0 \text{ mA}, I_B = -0.1 \text{ mA}$		-0.80	
V <sub>BE</sub> (sat)		I <sub>C</sub> = -10 mA, I <sub>B</sub> = -1.0 mA	-0.75	-0.95	V
		$I_C = -50 \text{ mA}, I_B = -5.0 \text{ mA}$		-1.50	
C <sub>ob</sub>	Output Capacitance	$V_{CB} = -5.0 \text{ V}, I_{E} = 0,$ f = 140 kHz		3.0	pF
C <sub>ib</sub>	Input Capacitance	V <sub>EB</sub> = -0.5 V, I <sub>C</sub> = 0, f = 140 kHz		3.5	pF
h <sub>fe</sub>	Small-Signal Current Gain	I <sub>C</sub> = -10 mA, V <sub>CE</sub> = -10 V, f = 100 MHz	8.5		/-
t <sub>s</sub>	Storage Time	$I_C$ = -10 mA, $V_{CC}$ = -1.5 V, $I_{B1}$ = $I_{B2}$ = -1.0 mA		20	ns
t <sub>on</sub>	Turn-On Time	$I_C = -10 \text{ mA}, V_{CC} = -1.5 \text{ V},$ $I_B = -1.0 \text{ mA}$		15	ns
t <sub>off</sub>	Turn-Off Time	$I_C = -10 \text{ mA}, V_{CC} = -1.5 \text{ V},$ $I_{B1} = I_{B2} = -1.0 \text{ mA}$		20	ns

#### Note:

4. Pulse test: pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2.0%.

# **Physical Dimensions**

## SOT-23 0.95 2.92±0.20 3 1.40 1.30<sup>+0.20</sup><sub>-0.15</sub> 2.20 0.60 0.37 (0.29) -0.95 ⊕ 0.20M A B 1.00 1.90 1.90 LAND PATTERN RECOMMENDATION 1.20 MAX SEE DETAIL A (0.93)0.10 ○ 0.10 M C C 2.40±0.30 NOTES: UNLESS OTHERWISE SPECIFIED **GAGE PLANE** A) REFERENCE JEDEC REGISTRATION TO-236, VARIATION AB, ISSUE H. B) ALL DIMENSIONS ARE IN MILLIMETERS. 0.23 0.08 C) DIMENSIONS ARE INCLUSIVE OF BURRS, 0.25 MOLD FLASH AND TIE BAR EXTRUSIONS. D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994. 0.20 MIN E) DRAWING FILE NAME: MA03DREV10 SEATING **PLANE** (0.55)

Figure 1. 3-LEAD, SOT23, JEDEC TO-236, LOW PROFILE (ACTIVE)

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**DETAIL A** 

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Definition of Terms			
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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.	
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